WHAT IS CLAIMED IS:

1. A driver circuit for driving a half bridge switching circuit, the driver circuit comprising:

an input trigger circuit receiving a pulsed input signal for controlling the generation of two drive signals, a first drive signal driving a high side switch of a half bridge switching circuit and a second drive signal driving a low side switch of the half bridge switching circuit;

a circuit for providing a dead time between the first and second drive signals whereby both the first and second drive signals are substantially zero;

the input trigger circuit generating a control signal for controlling the generation of the first and second drive signals based on a characteristic of the pulsed input signal; and

first and second drive circuits for providing said first and second drive signals.

2. The driver circuit of claim 1, wherein the characteristic of the pulsed input signal comprises a pulse edge of the pulsed input signal whereby when a pulse edge occurs, the first and second drive signals change state with said dead time between the drive signals.

3. The driver circuit of claim 2, wherein the characteristic comprises a rising edge.

4. The driver circuit of claim 2, wherein the input trigger circuit is non-responsive to a pulse duration of said pulsed input signal.

5. The driver circuit of claim 1, further comprising a shut down circuit receiving a shut down input for disabling the generation of said first and second drive signals.

6. The driver circuit of claim 1, wherein the pulsed input signal is generated by a microprocessor.

7. The driver circuit of claim 1, further comprising a circuit for generating said first and second drive signals with approximately a 50% duty cycle.

8. The driver circuit of claim 1, further comprising an under voltage lockout circuit for preventing generation of said first and second drive signals until the supply voltage for the driver circuit has stabilized.

9. The driver circuit of claim 1, further comprising a level shifting circuit for shifting a level of a signal driving at least one of said first and second drive circuits.

10. A ballast driver circuit for driving a switching circuit driving a gas discharge lamp, the ballast driver circuit comprising:

an input trigger circuit receiving a pulsed input signal for controlling the generation of two drive signals, a first drive signal driving a high side switch of a half bridge switching circuit and a second drive signal driving a low side switch of the half bridge switching circuit;

a circuit for providing a dead time between the first and second drive signals whereby both the first and second drive signals are substantially zero;

the input trigger circuit generating a control signal for controlling the generation of the first and second drive signals based on a characteristic of the pulsed input signal; and

first and second drive circuits for providing said first and second drive signals.

11. The ballast driver circuit of claim 10, wherein the characteristic of the pulsed input signal comprises a pulse edge of the pulsed input signal whereby when a pulse edge occurs, the first and second drive signals change state with said dead time between the drive signals.

12. The ballast driver circuit of claim 11, wherein the characteristic comprises a rising edge.

13. The ballast driver circuit of claim 11, wherein the input trigger circuit is non-responsive to a pulse duration of said pulsed input signal.

14. The ballast driver circuit of claim 10, further comprising a shut down circuit receiving a shut down input for disabling the generation of said first and second drive signals.

15. The ballast driver circuit of claim 10, wherein the pulsed signal is generated by a microprocessor.

16. The ballast driver circuit of claim 10, further comprising a circuit for generating said first and second drive signals with approximately a 50% duty cycle.

17. The ballast driver circuit of claim 10, further comprising an under voltage lockout circuit for preventing generation of said first and second drive signals until the supply voltage for the ballast driver circuit has stabilized.

18. The ballast driver circuit of claim 10, further comprising a level shifting circuit for shifting a level of a signal driving at least one of said first and second drive circuits.

19. A method for driving a half-bridge switching circuit comprising:

receiving a single pulsed input signal for controlling the generation of two drive signals, a first drive signal driving a high side switch of a half bridge switching circuit and a second drive signal driving a low side switch of the half bridge switching circuit;

providing a dead time between the first and second drive signals whereby both the first and second drive signals are substantially zero;

generating a control signal for controlling the generation of the first and second drive signals based on a characteristic of the pulsed input signal; and

generating the first and second drive signals.

20. The method of claim 19, wherein the step of generating a control signal comprises generating the control signal based on the location in time of a pulse edge of the pulsed input signal whereby when a pulse edge occurs, the first and second drive signals change state with said dead time between the drive signals.

21. The method of claim 20, wherein the characteristic comprises a rising edge.